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MOE, AUNG SOE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/327,523	Applicant(s) UENO ET AL.	
	Examiner Aung S. Moe	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed December 22, 2003 have been fully considered but they are not persuasive.

Regarding claims 1-3, 5-7, 12-14 and 15, the Applicant alleged that the prior art, e.g., Gowda '168, fails to show "a vertical scanning circuit is used for selecting pixels in units of rows by controlling a reset potential that is applied to selected reset switches."

In response, the Examiner respectfully disagrees because Gowda '168 clearly discloses the use of a vertical scanning circuit (i.e., noted that the Timing and Control Logic 14 is used to control the vertical scanning lines $15_1 - 15_N$ for controlling the vertical scanning of the imaging system 10; see col. 1, lines 45+ and col. 4, lines 30+) is used for selecting pixels (i.e., the pixel cells 30) in units of rows (i.e., noted that the buses RES/RSL are dedicated to pixels 30 in units of rows R1-RM as shown in Fig. 3A for selecting cells in units of rows; col. 4, lines 20-36) by controlling a reset potential that is applied to selected reset switches (i.e., as shown in Figs. 3A-3B, the reset switch 21 of the selected cells in units of rows R1-RM of the image sensor are controlled by the vertical scanning circuit 14 so that the reset potential applied to the reset switch 21 is controlled by the controller circuit 14 respectively. This is further evidenced from the time interval between t0 and t2 as shown in Figs. 5, 6 and 11; col. 4, lines 35+ and col. 5, lines 20+). In view of this, it is cleared as discussed in col. 4, lines 25+ of Gowda '168 that the pixel(s) selection function is carried out in conjunction with reset transistor 21 by controlling the reset

potential that is applied to the reset switches 21 of the selected ones of the pixels (i.e., the selected ones of cells 30) in units of rows (R1-RM) as required by the present claimed invention.

In view of the above, the Examiner continues to be of the opinion that Gowda '168 does in fact show the present claimed invention. Moreover, the newly added claims 16-21 are also rejected as being anticipated by Gowda '168, since Gowda '168 discloses the solid-state camera system and method comprising reading of a reference level with a falling edge of the reset pulse (as shown in Figs. 5, 6 and 11; col. 5, lines 15+ and col. 6, lines 5+), and wherein a changing state of reset pulse and a selection pulse initiates a pixel reading operation (i.e., col. 4, lines 20+, col. 5, lines 14+ and col. 6, lines 5+; see Figs. 5-6 and 11).

Drawings

1. The drawings (Figs. 7 and 18) were received on December 22, 2003. These drawings (Figs. 7 and 18) are approved by the Examiner. In view of these proposed drawing changes, the objection to the drawings as set forth in the previous office action is hereby withdrawn.

Claim Objections

1. Claim 2 is objected to because of the following informalities:

In claim 2, it is unclear how "a reset potential" recited in line 3 relates to "a reset potential" recited in claim 1, lines 9-10? If there are the same "reset potential", please change the words "a reset potential" as recited in line 3 of claim 2 to -- said reset potential - -.

In claim 2, it is unclear how "said reset switch**es**" recited in line 3 relates to either "a reset switch" as recited in claim 1, line 5 or "selected **ones of** said reset switch**es**" as recited in claim 1, line 10?

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-7, 12-14, 15 and 18-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Gowda et al. (U.S. 5,898,168).

Regarding claim 1, Gowda '168 discloses a solid-state imaging element (Figs. 2 and 3A), comprising: unit pixels (18/30), arranged in a matrix, each of which have photoelectric conversion element (26/110), transfer switch (Figs. 1 and 3B; the elements' 8 and 22; see col. 1, lines 30+ and col. 4, lines 20+) for transferring charge stored in said photoelectric conversion element (26), a charge store part (i.e., Figs. 1 and 3B; the elements' 7 and 25; col. 1, lines 65+ and col. 5, lines 50+) for storing charge transferred by said transfer switch (i.e., 8/22), a reset switch (Figs. 1 and 3B; the elements' 11 and 21) for resetting said charge store part (i.e., 7/25), and an amplifying element (i.e., Fig. 1 and 3B; the elements' 13 and 23; see col. 2, lines 10+) for outputting a signal in accordance with a potential of said charge in said charge store part (i.e., Figs. 1 and 3B; the element 15 and 15j);

a vertical scanning circuit (Figs. 2 and 3, the elements' 14 and 14') for selecting the pixels in units (18/30) of rows by controlling a reset potential applied to selected ones of said reset switches (11/21; see Figs. 5-6 and 11 and col. 4, lines 30+);

a horizontal scanning circuit (Figs. 2 and 3A; the elements' 28 and 31_1 to 31_N; col. 1, lines 50+ col. 4, lines 15+, and col. 5, lines 30+) for sequentially selecting signals output to said vertical signal lines (15/15j) (i.e., see col. 4, lines 35+); and

an output circuit (i.e., Figs. 2 and 3A; the elements' 31_1 to 31_N and 16; col. 1, lines 50+ and col. 6, lines 8+) for outputting signals selected by said horizontal scanning circuit (i.e., noted the bus lines connected between the elements 28 and 31 as shown in Figs. 2 and 3A).

Regarding claim 2, Gowda '168 discloses wherein said vertical scanning circuit applies vertical selection pulses sequentially output during vertical scanning to said reset switches as the reset potential thereof (i.e., see col. 4, lines 30+ and col. 5, lines 15+).

Regarding claim 3, Gowda '168 discloses wherein said charge stored part is floating diffusion (i.e., col. 1, lines 65+).

Regarding claim 5, Gowda '168 discloses wherein said output circuit outputs signals read into said vertical signal lines (15/15j) in voltage mode (i.e., "VOUT"; see col. 8, lines 20-25).

Regarding claim 6, Gowda '168 discloses wherein said output circuit outputs signals read into said vertical signal lines in current mode (i.e., col. 7, lines 39+).

Regarding claim 7, Gowda '168 discloses wherein said unit pixels (18/30) include an overflow (i.e., Fig. 14; the element 92) path between said photoelectric conversion element (26/110) and an area to which a pixel source voltage is applied (i.e., VDD), said overflow path being used to discharge excess charges of said photoelectric conversion element (i.e., col. 10, lines 15-32).

Regarding claim 12, Gowda '168 discloses a method for driving a solid-state imaging element (Figs. 2 and 3A) which includes unit pixels, arranged in a matrix (18/30), each of which have photoelectric conversion element (6/26/110), a transfer switch (8/22) for transferring charge stored in said photoelectric conversion element (6/26/110), charge stored part for storing charge (i.e., Figs. 1 and 3B; the elements' 7 and 25; col. 1, lines 65+ and col. 5, lines 50+) transferred by said transfer switch (8/22), reset switch (11/21) for resetting said charge store part (i.e., 7/25),

and an amplifying element (i.e., 13/23) for outputting a signal in accordance with a potential of said charge store part (i.e., 15/15j), said method comprising the step of:

selecting pixels in units of rows by controlling a reset potential applied to selected one of said reset switches (i.e., see Figs. 5-6 and 11; col. 4, lines 25+ and col. 5, lines 20+).

Regarding claim 13, Gowda '168 discloses the step of: outputting signals read into said vertical signal lines in voltage mode (i.e., col. 8, lines 21+).

Regarding claim 14, Gowda '168 discloses the step of: outputting signals read into said vertical signal lines in current mode (i.e., col. 7, lines 39+).

Regarding claim 15, Gowda '168 discloses a camera system (i.e., col. 1, lines 20-25) using a solid-state imaging element as an imaging device, said solid-state imaging element (i.e., Figs. 2 an 3A), comprising:

unit pixels, arranged in a matrix (i.e., Figs. 2 and 3A; the elements 18 and 30), which have a photoelectric conversion element (6/26), a transfer switch (8/22) for transferring charge stored in said photoelectric conversion element (6/26), a charge stored part for storing charge (i.e., Figs. 1 and 3B; the elements' 7 and 25; col. 1, lines 65+ and col. 5, lines 50+) transferred by said transfer switch (8/22), a reset switch (11/21) for resetting said charge store part (7/25), and amplifying elements (13/23) for outputting a signal in accordance with the potential of said charge store part (15/15j);

a vertical scanning circuit (Figs. 2 and 3, the elements' 14 and 14') for selecting pixels in units of rows (18/30) by controlling a reset potential applied to selected reset switches (11/21);

a horizontal scanning circuit (Figs. 2 and 3A; the elements' 28 and 31_1 to 31_N; col. 1, lines 50+ col. 4, lines 15+, and col. 5, lines 30+) for sequentially selecting signals output to said vertical signal lines in units of columns (i.e., see col. 4, lines 35+); and

an output circuit for outputting signals (i.e., Figs. 2 and 3A; the elements' 31_1 to 31_N and 16; col. 1, lines 50+ and col. 6, lines 8+) selected by said horizontal scanning circuit (i.e., noted the bus lines connected between the elements 28 and 31 as shown in Figs. 2 and 3A).

Regarding claim 16, Gowda '168 discloses the solid-state camera system and method comprising reading of a reference level with a falling edge of the reset pulse (as shown in Figs. 5, 6 and 11; col. 5, lines 15+ and col. 6, lines 5+).

Regarding claim 17, Gowda '168 discloses wherein a changing state of reset pulse and a selection pulse initiates a pixel reading operation (i.e., col. 4, lines 20+, col. 5, lines 14+ and col. 6, lines 5+; see Figs. 5-6 and 11).

Regarding claims 18-21, please see the Examiner's comments with respect to claims 16-17 as discussed above.

4. Claims 1-3, 6, 8, 12, and 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Fossum et al. (U.S. 5,949,483).

Regarding claim 1, Fossum '483 discloses a solid-state imaging element (Figs. 3A-3B, and 4; col. 5, lines 55+ and col. 6, lines 10+), comprising: unit pixels, arranged in a matrix (i.e., Figs. 4, 6A, 6B and 6C, the unit pixels 15, 502, 508 and 512), each of which have photoelectric

conversion element (i.e., Figs. 3A and 4; the elements' 30 and 15), a transfer switch for transferring charge (i.e., Fig. 3A, the element 35) stored in said photoelectric conversion element (30), a charge store part (i.e., the FD part 40 of Fig. 3A) for storing charge transferred by said transfer switch (i.e., see Fig. 3A; col. 6, lines 2+), a reset switch (i.e., Fig. 3A; the element 45) for resetting said charge store part (i.e., the FD part 40; see col. 6, lines 25+), and an amplifying element (i.e., Fig. 3A; the element 55; col. , lines 60-65 and col. 6, lines 5+) for outputting signals in accordance with the potential of said charge store part (i.e., Figs. 3A and 4; col. 6, lines 2+);

a vertical scanning circuit (Fig. 4, the row select circuit 18) for selecting the pixels in units of rows (i.e., noted from Figs. 3B and 6A-6C that the circuit 18 is used to select the pixels in units of rows as claimed; col. 10, lines 15+ and col. 11, lines 15+) by controlling a reset potential applied to selected ones of said reset switches (i.e., Noted that the reset switch 45 is respectively controlled by applying the respective potential to the selected ones of the reset switches which are selected by the controlling unit 18; see col. 6, lines 10+);

a horizontal scanning circuit (Fig. 3B, 7 and 8; the elements' 19, 21, 604, 610 and 612) for sequentially selecting signals output to said vertical signal lines (i.e., col. 9, lines 55+ and col. 10, lines 1-11); and

an output circuit (Fig. 3B, 7-8, 11 and 12, the elements 70, 21, 604) for outputting signals selected by said horizontal scanning circuit (i.e., col. 6, lines 55+, col. 9, lines 55+ and col. 10, lines 1+).

Regarding claim 2, Fossum '483 discloses wherein said vertical scanning circuit (Figs. 3A and 3B; the element's 18) applied vertical selection pulses sequentially output during vertical scanning to said reset switch as a reset potential thereof (i.e., col. 6, lines 10+ and col. 9, lines 40+).

Regarding claim 3, Fossum '483 discloses wherein said charge stored part is floating diffusion (col. 6, lines 14+).

Regarding claim 6, Fossum '483 discloses wherein said output circuit outputs signals read into said vertical signal lines in current mode (i.e., col. 3, lines 30+).

Regarding claim 8, Fossum '483 discloses wherein a negative potential is applied to the control electrode of each of said transfer switches (i.e., col. 6, lines 10+).

Regarding claim 12, Fossum '483 discloses a method for driving a solid-state imaging element (Figs. 3A-3B, and 4; col. 5, lines 55+ and col. 6, lines 10+) including unit pixels, arranged in a matrix (i.e., Figs. 4, 6A, 6B and 6C, the unit pixels 15, 502, 508 and 512), each of which have photoelectric conversion element (i.e., Figs. 3A and 4; the elements' 30 and 15), a transfer switch for transferring charge (i.e., Fig. 3A, the element 35) stored in said photoelectric conversion element (30), a charge store part (i.e., the FD part 40 of Fig. 3A) for storing charge transferred by said transfer switch (i.e., see Fig. 3A; col. 6, lines 2+), a reset switch (i.e., Fig. 3A; the element 45) for resetting said charge store part (i.e., the FD part 40; see col. 6, lines 25+), and an amplifying element (i.e., Fig. 3A; the element 55; col. , lines 60-65 and col. 6, lines 5+) for

outputting signals in accordance with the potential of said charge store part (i.e., Figs. 3A and 4; col. 6, lines 2+), said method comprising the step of:

selecting pixels in units of rows (i.e., noted from Figs. 3B and 6A-6C that the circuit 18 is used to select the pixels in units of rows as claimed; col. 10, lines 15+ and col. 11, lines 15+) by controlling a reset potential applied to selected ones of said reset switches (Noted that the reset switch 45 is respectively controlled by applying the respective potential to the selected ones of the reset switches which are selected by the controlling unit 18; see col. 6, lines 10+).

Regarding claim 14, Fossum '483 discloses the step of: outputting signals read into said vertical signal lines in current mode (i.e., col. 3, lines 25-30).

Regarding claim 15, Fossum '483 discloses a camera system using a solid-state imaging element as an imaging device (Figs. 3A-3B and 4), said solid-state imaging element, comprising:

unit pixels, arranged in a matrix (i.e., Figs. 4, 6A, 6B and 6C, the unit pixels 15, 502, 508 and 512), each of which have photoelectric conversion element (i.e., Figs. 3A and 4; the elements' 30 and 15), a transfer switch for transferring charge (i.e., Fig. 3A, the element 35) stored in said photoelectric conversion element (30), a charge store part (i.e., the FD part 40 of Fig. 3A) for storing charge transferred by said transfer switch (i.e., see Fig. 3A; col. 6, lines 2+), a reset switch (i.e., Fig. 3A; the element 45) for resetting said charge store part (i.e., the FD part 40; see col. 6, lines 25+), and an amplifying element (i.e., Fig. 3A; the element 55; col. , lines 60-65 and col. 6, lines 5+) for outputting signals in accordance with the potential of said charge store part (i.e., Figs. 3A and 4; col. 6, lines 2+);

a vertical scanning circuit (Fig. 4, the row select circuit 18) for selecting the pixels in units of rows (i.e., noted from Figs. 3B and 6A-6C that the circuit 18 is used to select the pixels in units of rows as claimed; col. 10, lines 15+ and col. 11, lines 15+) by controlling a reset potential applied to selected ones of said reset switches (i.e., Noted that the reset switch 45 is respectively controlled by applying the respective potential to the selected ones of the reset switches which are selected by the controlling unit 18; see col. 6, lines 10+);

a horizontal scanning circuit (Fig. 3B, 7 and 8; the elements' 19, 21, 604, 610 and 612) for sequentially selecting signals output to said vertical signal lines in units of columns (i.e., col. 9, lines 55+ and col. 10, lines 1-11); and

an output circuit for outputting signals (Fig. 3B, 7-8, 11 and 12, the elements 70, 21, 604) selected by said horizontal scanning circuit via horizontal signal lines (i.e., col. 6, lines 55+, col. 9, lines 55+ and col. 10, lines 1+).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
This application currently names joint inventors.

In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda '168 in view of Miwada (U.S. 5,206,932).

Regarding claim 4, it is noted that Gowda '168 does not explicitly state that the reset switches are depression type transistors.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Miwada '932. In particular, Miwada '932 teaches the use of depression type transistors in the solid-state imaging device as reset switches (Fig. 1; col. 4, lines 50-55) for resetting the floating diffused region (7) so that deterioration of the dynamic range is prevented (i.e., see col. 3, lines 1-5).

In view of the above, having the system of Gowda '168 and then given the well-established teaching of Miwada '932, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Gowda '168 as taught by

Miwada '932, since Miwada '932 states at column 3, lines 3+ that such a modification would prevent the solid-state imaging device from deterioration of the dynamic range resulting from faulty resetting of the floating diffused region thereof.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Roberts '004 shows a solid-state imaging device for selecting pixels in units of rows by controlling a reset potential of the reset switches (i.e., see Fig. 2 and 6)

Yonemoto '541 shows a solid-state imaging device using the reset switches for reading of a reference level with a falling edge of the reset pulse (Fig. 2), and wherein a changing state of the reset pulse and a selection pulse initiates a pixel reading operation (Fig. 4).

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aung S. Moe whose telephone number is 703-306-3021. The examiner can normally be reached on Mon-Fri (9-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aung S. Moe
Primary Examiner
Art Unit 2612

A. Moe
February 25, 2004